ORIGINAL

U.S. DISTRICT COURT
NORTHERN DISTRICT OF TEXAS
FILED
FEB 24 2005
CLERK, U.S. DISTRICT COURT
By _____ Deputy

UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF TEXAS
WICHITA FALLS DIVISION

WICHITA FALLS POWER MANAGEMENT, LLC, Plaintiff,	§	
	§	CIVIL ACTION NO.
v.	§	7-05CV-049-R
INTEL CORPORATION, Defendant.	§	**JURY TRIAL DEMANDED**

PLAINTIFF'S ORIGINAL COMPLAINT

Wichita Falls Power Management, LLC ("Wichita Falls Power Management" or "Plaintiff") files this Plaintiff's Original Complaint against Intel Corporation ("Intel" or "Defendant") as follows:

NATURE OF THE ACTION

1. This is a patent infringement action to stop Defendant's infringement of U.S. Patent No. 6,490,688. Plaintiff seeks injunctive relief and monetary damages. The patent-in-suit pertains to reducing power usage in microprocessor devices.

PARTIES

2. Plaintiff Wichita Falls Power Management, LLC is a Texas limited liability company. Plaintiff maintains its principal office at 807 Eighth Street, Suite 901, Wichita Falls, Texas 76301.

3. Defendant Intel Corporation is a corporation duly organized under the laws of the State of Delaware, with its principal place of business located at 2200 Mission College Boulevard, Santa Clara, California. Intel may be served via its registered agent for service of Process, CT Corporation System, 350 N. St. Paul Street, Dallas, Texas 75201.

JURISDICTION AND VENUE

4. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1 et seq., and in particular 35 U.S.C. §§ 271, 281, 283, 284, and 285. This Court has subject matter jurisdiction over this action under 28 U.S.C. §§ 1331 and 1338(a).

5. The Court has personal jurisdiction over Defendant because: Defendant has minimum contacts with the State of Texas and the Northern District of Texas; Defendant has purposefully availed itself of the privileges of conducting business in the State of Texas and in the Northern District of Texas; Defendant has sought protection and benefit from the laws of the State of Texas; Defendant regularly conducts business within the State of Texas and within the Northern District of Texas; and Plaintiff's causes of action arise directly from Defendant's business contacts and other activities in the State of Texas and in the Northern District of Texas. Defendant, directly or through intermediaries, ships, distributes, offers for sale, sells, and advertises its products and/or services in and to the State of Texas and the Northern District of Texas, specifically including the infringing products at issue in this suit. Defendant has committed acts of patent infringement in the State of Texas and in the Northern District of Texas, has contributed to acts of patent infringement in the State of Texas and in the Northern District of Texas, and/or has induced others to commit acts of patent infringement in the State of Texas and in the Northern District of Texas. Defendant maintains a registered agent in the State of Texas and in the Northern District of Texas.

6. Venue is proper in the Northern District of Texas under 28 U.S.C. §§ 1391 (b)-(c) and 1400(b) because Defendant committed substantial acts of infringement in this Judicial District and because Defendant is subject to personal jurisdiction in this Judicial District.

COUNT I - PATENT INFRINGEMENT

7. US. Patent No.6,490,688 (the "'688 patent"), entitled "Process and Apparatus for Reducing Power Usage in Microprocessor Devices According to the Type of Activity Performed by the Microprocessor," was duly and legally issued by the United States Patent and Trademark Office on December 3, 2002 after full and fair examination. Plaintiff was assigned the '688 patent and continues to hold all rights and interest in the '688 patent, specifically including the right to sue for patent infringement. A true and correct copy of the '688 patent is attached hereto as **Exhibit "A."**

8. Defendant has infringed and is infringing the '688 patent. The infringing acts include, but are not limited to, the manufacture, use, sale, importation, and/or offer for sale of microprocessors utilizing Intel's "XScale" microarchitecture and practice of the methods claimed in the '688 patent; inducing and contributing to the manufacture, use, sale, importation, and/or offer for sale of computer systems based upon microprocessors utilizing Intel's "XScale" microarchitecture and the practice of methods claimed in the '688 patent; and the manufacture, use, sale, importation and/or offer for sale of microprocessors utilizing Intel's "XScale" microarchitecture knowing them to be especially made or especially adapted for use in an infringement of said patent.

9. Defendant's aforesaid activities have been without authority and/or license from Plaintiff. Upon information and belief, Defendant's infringement of the patent-in-suit is willful and deliberate.

10. Defendant's acts of infringement have caused damage to Plaintiff. Plaintiff is likely to be irreparably harmed by Defendant's infringement, inducement to infringe, and contributory infringement of the '688 patent unless enjoined by this court. Plaintiff is entitled to relief for such infringement pursuant to 35 U.S.C. §§ 283 and 284.

JURY DEMAND

11. Plaintiff demands a trial by jury on all issues.

RELIEF

Plaintiff Wichita Falls Power Management respectfully requests the following relief:

A. that the Court adjudge that Defendant has infringed the '688 patent;

B. that the Court issue a permanent injunction enjoining Defendant from making, using, selling, or offering for sale in the United States any products or services, and from undertaking processes, embodying the patented inventions claimed in the '688 patent;

C. that the Court award damages to Plaintiff to which it is entitled;

D. that the Court treble the damages for Defendant's willful infringement as provided for in 35 U.S.C. § 284;

E. that the Court award interest on such damages;

F. that the Court award Plaintiff's costs and attorneys' fees incurred in this action; and,

G. that the Court award such other relief as the Court deems just and proper.

Respectfully submitted,

By: _____

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ATTORNEYS FOR PLAINTIFF WICHITA FALLS POWER MANAGEMENT, LLC

(12) **United States Patent**
Rosch

(10) **Patent No.: US 6,490,688 B2**
(45) **Date of Patent: *Dec. 3, 2002**

(54) **PROCESS AND APPARATUS FOR REDUCING POWER USAGE IN MICROPROCESSOR DEVICES ACCORDING TO THE TYPE OF ACTIVITY PERFORMED BY THE MICROPROCESSOR**

(76) Inventor: **Winn L. Rosch**, 20,000 Shaker Blvd., Shaker Heights, OH (US) 44122

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/873,764**

(22) Filed: **Jun. 4, 2001**

(65) **Prior Publication Data**

US 2002/0069372 A1 Jun. 6, 2002

Related U.S. Application Data

(63) Continuation of application No. 08/494,021, filed on Jun. 23, 1995, now Pat. No. 6,243,820, which is a continuation of application No. 08/320,566, filed on Oct. 11, 1994, now abandoned, which is a continuation of application No. 08/080,578, filed on Jun. 21, 1993, now abandoned, which is a continuation of application No. 07/954,706, filed on Sep. 30, 1992, now Pat. No. 5,222,239, which is a continuation of application No. 07/387,341, filed on Aug. 28, 1989, now abandoned.

(51) **Int. Cl.**[7] **G06F 1/32**
(52) **U.S. Cl.** **713/322**; 713/600
(58) **Field of Search** 713/300–340, 713/600–601

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,381,552	A *	4/1983	Nocilini et al.	365/227
4,819,164	A *	4/1989	Branson	713/501
4,851,987	A *	7/1989	Day	365/227
4,893,271	A *	1/1990	Davis et al.	365/227
5,142,684	A *	8/1992	Perry et al.	709/102
5,428,790	A *	6/1995	Harper et al.	713/322
5,495,617	A *	2/1996	Yamada	713/323

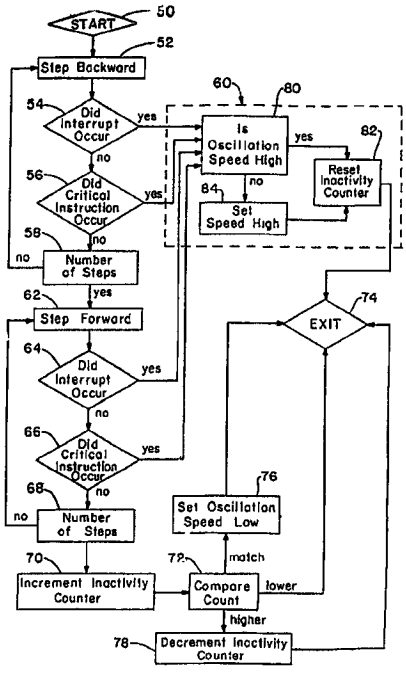
* cited by examiner

Primary Examiner—Sumati Lefkowitz
(74) *Attorney, Agent, or Firm*—Ward & Olivo

(57) **ABSTRACT**

A process and apparatus for preparing the process for reducing the power consumption of microprocessor-based devices by reducing the frequency of the oscillator governing the logical operation of the microprocessor during periods of use in which system performance is not critical. In one embodiment of the apparatus, the microprocessor is controlled by a monitor circuit operable with the microprocessor and operated by the variable frequency oscillator. In another embodiment a hardware monitor circuit is utilized and which tracks microprocessor instructions to determine periods of use when performance is not critical. The shift in oscillator speed is mediated by a flip-flop latch circuit connected between one or more clock oscillators and the oscillator input of the controlled microprocessor.

6 Claims, 2 Drawing Sheets



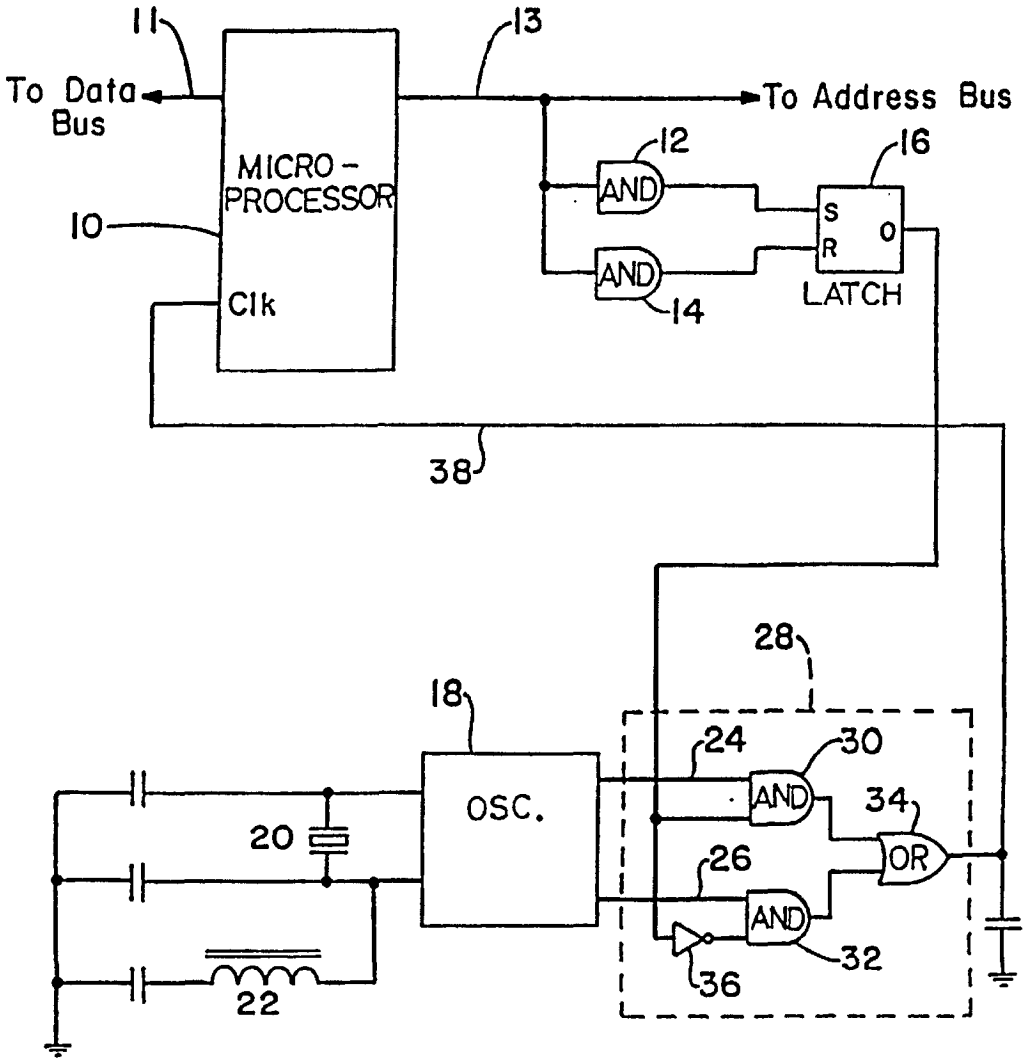
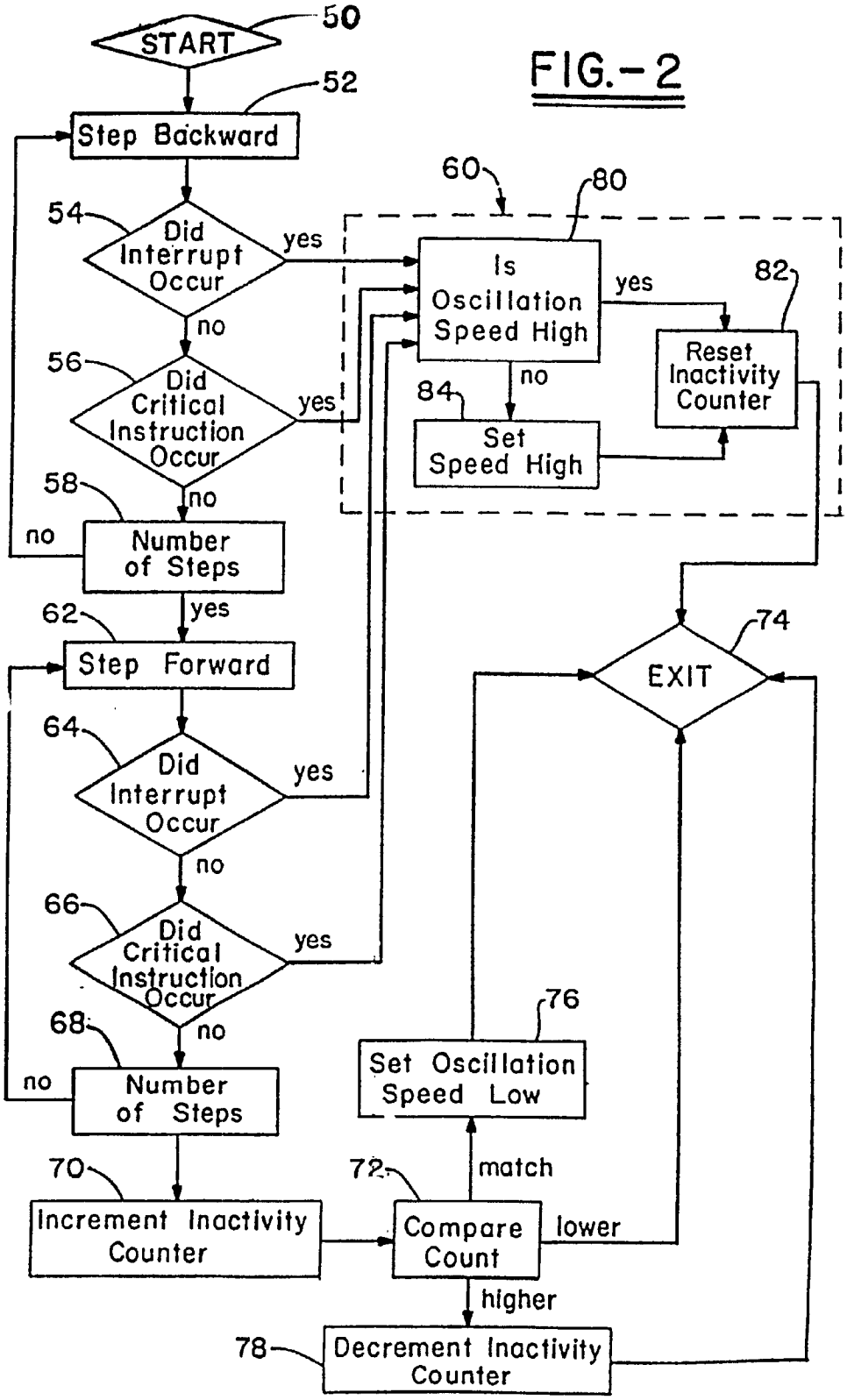

11
To Data Bus
MICRO-PROCESSOR
10
Clk
13
To Address Bus
12
AND
AND
14
16
S
R
Q
LATCH
38
28
18
OSC.
20
22
24
30
AND
34
OR
26
AND
32
36

FIG.-1

FIG.-2


START
50
52
Step Backward
60
80
54
Did Interrupt Occur
yes
no
Is Oscillation Speed High
yes
82
Reset Inactivity Counter
56
Did Critical Instruction Occur
yes
no
84
Set Speed High
58
no
Number of Steps
no
yes
62
Step Forward
74
EXIT
64
Did Interrupt Occur
yes
no
66
Did Critical Instruction Occur
yes
no
76
Set Oscillation Speed Low
68
no
Number of Steps
70
72
match
Increment Inactivity Counter
Compare Count
lower
higher
78
Decrement Inactivity Counter

PROCESS AND APPARATUS FOR REDUCING POWER USAGE IN MICROPROCESSOR DEVICES ACCORDING TO THE TYPE OF ACTIVITY PERFORMED BY THE MICROPROCESSOR

This application is a continuation of application Ser. No. 08/494,021 filed on Jun. 23, 1995, now U.S. Pat. No. 6,243,820, which is a continuation of Ser. No. 08/320,566 filed on Oct. 11, 1994, now abandoned, which is a continuation of Ser. No. 08/080,578 filed on Jun. 21, 1993, now abandoned, which is a continuation of Ser. No. 07/954,706 filed on Sep. 30, 1992, now U.S. Pat. No. 5,222,239, which is a continuation of Ser. No. 07/387,341 filed on Aug. 28, 1998, now abandoned.

TECHNICAL FIELD

The present invention relates to a method and apparatus for reducing power consumption of a microprocessor based device which is designed to operate from a stored energy source so as to extend the useful life of the stored energy source and therefore the ability to use the microprocessor based device. More particularly, the invention relates to a method and apparatus which reduces the power usage of the microprocessor itself during periods of inactivity or where the full extent of the microprocessor's capabilities are not necessary for the tasks being performed on the device. The reduction in power usage of the microprocessor is accomplished automatically based upon determinations of such inactivity or other predetermined conditions.

BACKGROUND OF THE INVENTION

There are a growing number of portable microprocessor-based devices such as laptop computers, which are designed to run on batteries far from utility lines. In these systems, power consumption has been a primary factor limiting system design. Without adequate battery life, normal processing tasks cannot be completed in the operating time available. Consequently, most aspects of the design of portable microprocessor-based devices have been optimized to conserve battery power. The power required by display systems, disk memory, and support circuitry have all been reduced. The known methods used to conserve power are two: first, to develop components that consume less power, and second, to interrupt or suspend component operation during period's of inactivity. These two methods are effective for all components except the microprocessor itself.

Power savings have been achieved in display systems by the above two strategies. The technologies used for screen displays have shifted from those consuming large power such as cathode ray tube, light emitting diode, and gas-plasma displays, to those with more modest power requirements, principally liquid crystal displays with or without backlighting. In addition, circuitry has been introduced to microprocessor-based devices to automatically shut off the screen, thereby conserving the power that it would use during lengthy periods of system inactivity.

Inactivity is typically determined by the absence of change in the data displayed on the screen or typed at the keyboard of a microprocessor-based device. The power consumed by disk drives has been reduced by using newer designs that are smaller and more energy efficient. In addition, hard disk drives, which normally consume power continuously because their magnetic media must be kept constantly spinning, have been devised which automatically stop their rotation after a predetermined period of

microprocessor-based device inactivity. Inactivity is determined by the absence of commands to store data on or retrieve data from the storage medium.

Although these steps have helped to extend the usefulness of portable microprocessor-based devices, there has also been a trend to put increasingly powerful microprocessors into the machines. This exacerbates the battery power drain because more powerful microprocessor-based devices are more complicated, have more internal circuitry, and naturally consume more energy. For example, the Intel 80386 microprocessor comprises about 375,000 separate internal transistors; the newer 80486 comprises over a million, and even newer devices in the future will necessarily be comprised of even larger numbers.

Microprocessor power reduction has been achieved in some portable microprocessor-based devices such as those based on the 8088 and 80286 made by Intel Corporation by using special designs based on low-power Complementary Metal Oxide (CMOS) semiconductor technology, which is an inherently more power-efficient technology than other common semiconductor technologies. As a result, the power required by the microprocessor in such devices is not as large a fraction of the total power required by the entire microprocessor-based system.

However, the more powerful the microprocessor, the greater the fraction of system power resources must be devoted to its operation. The 80386 microprocessor, for instance, can consume five to eight watts, which is more than the total consumption of all the circuitry and components in a less powerful microprocessor-based device combined. Yet more powerful portable microprocessor-based devices, such as those based on the Intel 80386 and other advanced designs already use CMOS internal circuitry. The effects of utilizing more powerful microprocessors such as the Intel 80386 can be seen in one known portable lap-top computer utilizing the 80386 microprocessor which will have a typical operatic time of ½ hour before the battery life of the device is exhausted. This assumes that the computer is being used, At least to some degree, for computing tasks which will consume more power than the simple house keeping functions of the microprocessor. In the known laptop computer, the microprocessor is operated at a relatively slow speed of 12.5 MHz., to try and extend the useful life of the device, but also results in non-efficient operation of the device.

Moreover, the other traditional power saving techniques cannot be applied to the microprocessor. The microprocessor cannot be stopped during periods of inactivity. When the microprocessor stops its operation, the microprocessor-based device itself stops operating and is unable to detect when to resume operation when activity is resumed. Also as mentioned before, the microprocessor is never completely inactive. In all practical microprocessor-based devices, the microprocessor constantly engages in housekeeping functions. It continuously executes instructions to monitor the data-input devices, such as sensors or keyboards, as well as its input and output ports for new data input.

This monitoring process typically involves repeatedly executing a looping string of instructions. Stopping the operation of the microprocessor would halt the execution of those instructions necessary for monitoring the system, depriving the microprocessor of the ability to restart itself. Consequently, all current portable microprocessor-based devices must necessarily keep the microprocessor operating at all times.

It is also recognized that the power consumed by a microprocessor is directly related to the frequency of the

oscillator driving it. During normal operation, the circuitry inside a microprocessor is constantly active· transistors continuously change state to execute logic operations as governed by the oscillator. Each change of state necessarily consumes a fixed and predetermined amount of power. The more often state changes take place; the more power is consumed by the microprocessor. On the other hand, reducing the oscillator speed also degrades the data processing ability of the microprocessor, contrary to the primary design goal in using a more powerful microprocessor which is to improve performance through higher operations speeds. Thus, unfortunately, the consequence of greater microprocessor speed, and better, more desirable performance characteristics, is greater power consumption

There are also known in the prior art computers and other devices which are capable of multi-speed operation such is found with a "turbo" function associated with some personal computers. These devices essentially operate at a normal operating speed under most circumstances but may be changed to operate at a higher speed for compatibility with software which is speed critical. In order to change the operating speed in these devices, a switch or instruction given by the user through the keyboard or other input device will manually convert the speed of operation dependent upon the user requirements. In such a system, the multi-speed operation does not reflect upon power usage of the device as such devices are not designed to be portable and run from a battery or other stored energy source.

SUMMARY OF THE INVENTION

Based upon the foregoing, it is a main object of the invention is to reduce the power consumption of microprocessor. Based devices through the application of a specific process and apparatus to perform said process which reduces the frequency of the oscillator driving the microprocessor automatically during the periods in which it is performing non-critical operations. That is, microprocessor speed reduction during periods in which all of the-data processing ability of the microprocessor-based device is not demanded.

It is another object of the invention to provide a method of reducing the power consumption of a microprocessor-based device wherein the microprocessor itself is utilized to determine periods of inactivity or other predetermined conditions to reduce the microprocessors operating speed accordingly.

It is yet another object of the invention to provide the process and apparatus to reduce the power consumption of a microprocessor-based device by utilization of an external circuit which-may be incorporated into the device to determine periods of inactivity or other predetermined conditions to reduce the operating speed automatically.

A further object of the invention is to provide a method and apparatus to reduce the power consumption of a microprocessor-based device which utilizes the occurrence of critical instructions or non-critical instructions or the reoccurrence of non-critical instructions to determine periods of activity or inactivity respectively, from which the operating speed of the device may be automatically changed accordingly.

These and other Objects are realized using the apparatus of the present invention which may be comprised of three parts in addition to the typical circuitry of a microprocessor-based device: a monitoring module, an oscillator latch, and a source of multiple oscillator frequencies.

The monitoring module may be implemented either as a defined process running on an unmodified microprocessor

such as the Intel 80386 (or any improved future microprocessor design), as a hardware circuit connected to the data lines of this or any other microprocessor, or as a hardware code internalized inside the microprocessor.

The monitoring module may serve the functions of determining periods of non-critical use and the onset of critical use of the microprocessor. Periods of non-critical use are determined by the lapse of a predetermined time period without the occurrence of a critical defined command (specific interrupts or other predetermined instructions) or the repetition of a pattern of non-critical instructions for a given number of iterations (for example, instructions for polling a keyboard, parity-checking a spreadsheet, or polling sensor devices). The onset of critical use is determined by the occurrence of certain defined interrupts or instructions in the sequence read by the microprocessor.

The monitoring module controls a bi-state logic latch, the second part of the apparatus which selects between two sources for the oscillator frequency to be delivered to the microprocessor. When the latch receives an indication of critical use from the monitoring module, it selects the higher oscillator frequency. Alternatively, when it receives an indication of non-critical use, it selects the lower oscillator frequency.

In its most elementary form, the source of multiple oscillator frequencies is a standard oscillator circuit coupled to a simple frequency divider. Such a design assures that the two oscillator frequencies are constantly synchronized. More design freedom is afforded by using two separate, independently-operating oscillators, which need not be related in frequency. In this case, however, the oscillator latch must incorporate additional logic to match oscillator cycles to maintain an acceptable duty cycle during the switching period.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects and advantages of the present invention as well as the various embodiments and their operation will be more clearly understood with reference to the following detailed description in conjunction with the accompanying drawings, wherein:

FIG. **1** shows a particular implementation of the invention using a process running on the controlled microprocessor to determine operating speed, and

FIG. **2** is a flow chart of the monitor process for operating this system.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to the drawings, one embodiment as shown in FIG. **1**, includes a microprocessor **(10)**, such as an Intel 80386, which is conventionally connected to the memory and other circuitry of a microprocessor-based device through data ports coupled to the data bus of the device at **11**. The multiple-AND gates **(12)** and **(14)** are connected to the address lines of the microprocessor at **13**. Each gate monitors separate addresses generated by the microprocessor which represent a request for high-speed operation or low speed operation. These gates drive a set/reset latch **(16)** so that a logical high from gate **(12)** latches a high output from the latch **(16)** and a logical high from gate **(14)** resets the output of latch **(16)** low. Through addressing constraints, both gates **(12)** and **(14)** are prevented from being high simultaneously, avoiding error conditions. The output of latch **(16)** supplies the +HI/−LO signal for driving the speed latch to be subsequently described.

In the interrupt service routine as shown in FIG. 2, the microprocessor itself analyzes the instruction stream searching for an interrupt or critical instruction as described. The particular number of steps used in the searching routine is not critical and may be selected to provide optimum efficiency. A list of critical instructions for each family of microprocessors can be provided in a look up table which can be stored in memory such as a random access memory (RAM) or a read only memory (RAM) or anywhere that the microprocessor has access to such as list. Alternatively, an external processor may be provided having its own EPROM memory containing such a list or the list can be hard wired into the microprocessor chip itself. It should also be recognized that although the invention has been described with reference to a determination of an interrupt or critical instruction, the interrupt service routine can also operate to determine the occurrence or reoccurrence of a series of non-critical instructions which may indicate house keeping or other routine functions such as polling of the keyboard, parity checking or other similar functions.

The present invention thus provides a simple and yet effective way in which to reduce power consumption by a microprocessor and therefore of a microprocessor-based system which is operated from a stored energy source. As an example, a first oscillator frequency of 16 MHz. may be provided for high speed operation which may provide less than one hour of computing time due to depletion of a battery source utilized therewith. Utilizing this invention, a second oscillator frequency of 4 MHz. may be provided for low speed operation of the system during non-critical performance needs which will have the effect of extending the useful life of the system to over two hours under most circumstances. It is recognized that any operating frequencies may be provided for the particular tasks to be accomplished by the microprocessor-based system, such as for example a high speed operating frequency of 33 MHz. being the state of the art at the present time to a low speed operating frequency of 4 MHz. which is adequate for processing key strokes and the like. It can thus be seen that use of the present invention will extend the useful life of the microprocessor-based system easily by a factor of two or more from which the benefits should be apparent.

Although the present invention has been described with reference to a particular embodiment thereof, this is meant to be illustrative only and is not to be construed as limiting the scope of the invention. Various modifications and changes will occur to those skilled in the art without departing from the spirit and scope of the present invention as defined in the appended claims.

What is claimed is:

1. A process for automatically reducing the power usage of a microprocessor comprising the steps of:

continuously generating monitor interrupt signals for monitoring the operations of the microprocessor at predetermined intervals of time,

searching within an instruction stream of the microprocessor for a plurality of instructions executed by the microprocessor upon the occurrence each of said monitor interrupt signals by means of a monitoring circuit,

comparing said plurality of searched instructions with a predefined list of instructions stored in memory comprising wired connections to determine when at least one of said searched instructions constitutes a predefined instruction,

supplying at least a first operation frequency to said microprocessor upon the occurrence of said predefined instruction, and a reduced second operation frequency to said microprocessor upon the non-occurrence of said predefined instruction, wherein the power usage of said microprocessor is reduced according to the occurrence or non-occurrence of said predefined instruction by reduction of the operation frequency supplied to said microprocessor.

2. A process as in claim **1** wherein said comparing is performed by wired logic.

3. A process as in claim **2** wherein the result of said comparing is stored for later usage by the microprocessor.

4. A process for automatically reducing the power usage of a microprocessor comprising:

designating certain portions of the code being executed by the microprocessor as critical code,

providing for operating the microprocessor at two or more different clock frequencies,

periodically interrupting the microprocessor

determining whether the microprocessor was executing any of the said critical code in the interval prior to the interrupt,

selecting said microprocessor clock frequency such that the microprocessor is set to operate at a higher frequency when the microprocessor was executing any of said critical code in the interval prior to the interrupt, and at a lower frequency when the microprocessor was not executing any of said critical code in the interval prior to the interrupt.

5. A system containing a microprocessor comprising:

a clock frequency source capable of providing one of two or more frequencies to the microprocessor,

an interrupt service routine,

a circuit which periodically interrupts the microprocessor causing the microprocessor to execute said interrupt service routine,

a set of predefined instructions,

a predetermined range of time values,

said interrupt service routine determining whether said microprocessor had executed any of said predefined instructions within said predetermined range of time values prior to the interrupt,

said interrupt service routine also providing for selection of one of said clock frequencies taking into account said determination.

6. A system as in claim **5** wherein monitor hardware provides information about the execution of predetermined instructions to said interrupt service routine.

* * * * *

ORIGINAL

CIVIL COVER SHEET

The JS-44 civil cover sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. (SEE INSTRUCTIONS ON THE REVERSE OF THE FORM.)

FILED
FEB 24 2005
CLERK, U.S. DISTRICT COURT
NORTHERN DISTRICT OF TEXAS

I.(a) PLAINTIFF

WICHITA FALLS POWER MANAGEMENT, LLC a Texas Limited Liability Company

(b) COUNTY OF RESIDENCE OF FIRST LISTED PLAINTIFF WICHITA FALLS, TEXAS
(EXCEPT IN U.S. PLAINTIFF CASES)

DEFENDANT

INTEL CORPORATION, a Delaware Corporation

COUNTY OF RESIDENCE OF FIRST LISTED DEFENDANT SANTA CLARA, CA
(IN U.S. PLAINTIFF CASES ONLY)
NOTE: IN LAND CONDEMNATION CASES, USE THE LOCATION OF THE TRACT OF LAND INVOLVED.

(c) ATTORNEYS (FIRM NAME, ADDRESS, AND TELEPHONE NUMBER)
Thomas H Cook, Jr., Richard G. Urquhart, ZELLE, HOFMANN, VOELBEL, MASON & GETTE, L L P. , 1201 Main Street, Suite 3000, Dallas, Texas 75202, 214-742-3000

ATTORNEYS (IF KNOWN) 7-05CV-049-

II. BASIS OF JURISDICTION (PLACE AN "X" IN ONE BOX ONLY)

- ☐ 1 U.S GOVERNMENT Plaintiff
- ☒ 3 FEDERAL QUESTION (U.S. Government Not a Party)
- ☐ 2 U.S. GOVERNMENT Defendant
- ☐ 4 DIVERSITY (Indicate Citizenship of Parties in Item III)

III. CITIZENSHIP OF PRINCIPAL PARTIES (FOR DIVERSITY CASES ONLY) (PLACE AN "X" IN ONE BOX FOR PLAINTIFF AND ONE BOX FOR DEFENDANT)

	PTF	DEF		PTF	DEF
Citizen of This State	☐ 1	☐ 1	Incorporated *or* Principal Place of Business In This State	☐ 4	☐ 4
Citizen of Another State	☐ 2	☐ 2	Incorporated *and* Principal Place of Business in Another State	☐ 5	☐ 5
Citizen or Subject of a Foreign Country	☐ 3	☐ 3	Foreign Nation	☐ 6	☐ 6

IV. NATURE OF SUIT (PLACE AN "X" IN ONE BOX ONLY)

CONTRACT

- ☐ 110 Insurance
- ☐ 120 Marine
- ☐ 130 Miller Act
- ☐ 140 Negotiable Instrument
- ☐ 150 Recovery of Overpayment & Enforcement of Judgment
- ☐ 151 Medicare Act
- ☐ 152 Recovery of Defaulted Student Loans (Excl Veterans)
- ☐ 153 Recovery of Overpayment of Veteran's Benefits
- ☐ 160 Stockholders' Suits
- ☐ 190 Other Contract
- ☐ 195 Contract Product Liability

TORTS

PERSONAL INJURY
- ☐ 310 Airplane
- ☐ 315 Airplane Product Liability
- ☐ 320 Assault, Libel and Slander
- ☐ 330 Federal Employers' Liability
- ☐ 340 Marine
- ☐ 345 Marine Products Liability
- ☐ 350 Motor Vehicle
- ☐ 355 Motor Vehicle Product Liability
- ☐ 360 Other Personal Injury

PERSONAL INJURY
- ☐ 362 Personal Injury -- Med Malpractice
- ☐ 365 Personal Injury -- Product Liability
- ☐ 368 Asbestos Personal Injury Product Liability

PERSONAL PROPERTY
- ☐ 370 Other Fraud
- ☐ 371 Truth in Lending
- ☐ 380 Other Personal Property Damage
- ☐ 385 Property Damage Product Liability

FORFEITURE/PENALTY

- ☐ 610 Agriculture
- ☐ 620 Other Food & Drug
- ☐ 625 Drug Related Seizure of Property 21 USC 881
- ☐ 630 Liquor Laws
- ☐ 640 R R & Truck
- ☐ 650 Airline Regs.
- ☐ 660 Occupational Safety/Health
- ☐ 680 Other

BANKRUPTCY

- ☐ 422 Appeal 28 USC 158
- ☐ 423 Withdrawal 28 USC 157

PROPERTY RIGHTS

- ☐ 820 Copyrights
- ☒ 830 Patent
- ☐ 840 Trademarks

OTHER STATUTES

- ☐ 400 State Reapportionment
- ☐ 410 Antitrust
- ☐ 430 Banks and Banking
- ☐ 450 Commerce/ICC Rates/etc
- ☐ 460 Deportation
- ☐ 470 Racketeer influenced and Corrupt Organizations
- ☐ 810 Selective Service
- ☐ 850 Securities/Commodities/ Exchange
- ☐ 875 Customer Challenge 12 USC 3410
- ☐ 891 Agricultural Acts
- ☐ 892 Economic Stabilization Act
- ☐ 893 Environmental Matters
- ☐ 894 Energy Allocation Act
- ☐ 895 Freedom of Information act
- ☐ 900 Appeal of Fee Determination Under Equal Access to Justice
- ☐ 950 Constitutionality of State Statutes
- ☐ 990 Other Statutory Actions

REAL PROPERTY

- ☐ 210 Land Condemnation
- ☐ 220 Foreclosure
- ☐ 230 Rent Lease & Ejectment
- ☐ 240 Torts to Land
- ☐ 245 Tort Product Liability
- ☐ 290 All Other Real Property

CIVIL RIGHTS

- ☐ 441 Voting
- ☐ 442 Employment
- ☐ 443 Housing/ Accommodations
- ☐ 444 Welfare
- ☐ 445 Other Civil Rights

PRISONER PETITIONS

- ☐ 510 Motions to Vacate Sentence HABEAS CORPUS:
- ☐ 530 General
- ☐ 535 Death Penalty
- ☐ 540 Mandamus & Other
- ☐ 550 Civil Rights
- ☐ 555 Prison Condition

LABOR

- ☐ 710 Fair Labor Standards Act
- ☐ 720 Labor/Mgmt Relations
- ☐ 730 Labor/Mgmt Reporting & Disclosure Act
- ☐ 740 Railway Labor Act
- ☐ 790 Other Labor Litigation
- ☐ 791 Empl Ret. Inc Security Act

SOCIAL SECURITY

- ☐ 861 HIA (1395(l))
- ☐ 862 Black Lung (823)
- ☐ 863 DIWC/DIWW (405(g))
- ☐ 864 SSID Title XVI
- ☐ 865 RSI (405(g))

FEDERAL TAX SUITS

- ☐ 870 Texas (U S Plaintiff or Defendant)
- ☐ 871 IRS - Third Party 28 USC 7609

V. ORIGIN (PLACE AN "X" IN ONE BOX ONLY)

☒ 1 Original Proceeding | ☐ 2 Removed from State Court | ☐ 3 Remanded from Appellate Court | ☐ 4 Reinstated or Reopened | ☐ 5 Transferred from another district (specify) | ☐ 6 Multidistrict Litigation | ☐ 7 Appeal to District Judge from Magistrate Judgment

VI. CAUSE OF ACTION (CITE THE U S. CIVIL STATUE UNDER WHICH YOU ARE FILING AND WRITE BRIEF STATEMENT OF CAUSE. DO NOT CITE JURISDICTIONAL STATUTES UNLESS DIVERSITY)
Patent Infringement, 35 U S.C § , et seq , and in particular 35 U S C. §§ 271, 281, 283, 284 and 285; Subject Matter Jurisdiction under 28 U S C Secs 1331 and 1338(a).

VII. REQUESTED IN COMPLAINT: CHECK IF THIS IS A CLASS ACTION **DEMAND $** ☐ UNDER F.R.C.P. 23
CHECK YES only if demanded in complaint: **JURY DEMAND:** ☒ YES ☐ NO

VIII. RELATED CASE(S) IF ANY (See instructions): JUDGE _____ DOCKET NUMBER _____

DATE
February 23, 2005

SIGNATURE OF ATTORNEY OF RECORD

FOR OFFICE USE ONLY RECEIPT # 38542 AMOUNT 250.00 APPLYING IFP _____ JUDGE _____ MAG JUDGE _____

JS 44 Reverse
(Rev. 3/99)